WHAT IS CLAIMED IS:

1. A borderless contact structure comprising:

a semiconductor substrate having a top surface;

a device isolation region formed in a predetermined region of the semiconductor substrate, the device isolation region having a protrusion that is higher in level than the top surface of the semiconductor substrate;

an impurity diffusion region formed in an active region surrounded by the device isolation region;

an etch stop spacer formed overlying a sidewall of the protrusion;

an etch stop layer and an interlayer insulating layer sequentially formed over the resultant structure; and

a contact hole opening the interlayer insulating layer and the etch stop layer, the contact hole exposing at least a portion of the impurity diffusion region.

2. The borderless contact structure according to claim 1, wherein the etch stop spacer is partially etched.

3. The borderless contact structure according to claim 1, wherein the device isolation region comprises a trench isolation region.

4. The borderless contact structure according to claim 3, further comprising a thermal oxide layer interposed between the semiconductor substrate and the trench isolation region.

5. The borderless contact structure according to claim 4, further comprising a silicon nitride liner interposed between the trench isolation region and the thermal oxide layer.

6. The borderless contact structure according to claim 1, wherein the etch stop spacer comprises silicon nitride or silicon oxynitride.

7. The borderless contact structure according to claim 1, wherein the etch stop layer comprises silicon nitride or silicon oxynitride.

8. The borderless contact structure according to claim 1, further comprising an interconnection line filling the contact hole.

9. The borderless contact structure according to claim 1, further comprising:

a contact plug filling the contact hole; and

an interconnection line overlying the contact plug.

10. The borderless contact structure according to claim 1, wherein the contact hole exposes not only the impurity diffusion region but also a portion of the etch stop spacer adjacent to the exposed impurity diffusion region.

11. A method of forming a borderless contact structure, the method comprising:

selectively etching a predetermined portion of a semiconductor substrate to form a trench defining an active region having a top surface;

forming a device isolation region in the trench, the device isolation region having a protrusion which is higher in level than the top surface of the active region;

forming an etch stop spacer on a sidewall of the protrusion;

forming an impurity diffusion region in the active region;

sequentially forming an etch stop layer and an interlayer insulating layer over the resultant structure; and

successively patterning the interlayer insulating layer and the etch stop layer to form a contact hole exposing at least a portion of the impurity diffusion region.

12. The method according to claim 11, wherein the step of forming an etch stop spacer comprises:

forming a gate pattern on the active region;

forming a lightly doped drain (LDD) region in the active region at both sides of the gate pattern;

forming an insulating layer for for forming a spacer on the resultant structure including the LDD region, the insulating layer for forming a spacer being formed of a material having an etching selectivity with respect to the interlayer insulating layer; and

anisotropic etching the insulating layer for forming a spacer to form a gate spacer on a sidewall of the gate pattern and to form the etch stop spacer on the sidewall of the protrusion of the device isolation region.

13. The method according to claim 11, wherein the etch stop spacer is made of silicon nitride or silicon oxynitride.

14. The method according to claim 11, wherein the etch stop layer is made of silicon nitride or silicon oxynitride.

15. The method according to claim 11, further comprising:

forming a contact plug in the contact hole; and

forming an interconnection line overlying the contact plug.

16. The method according to claim 11, wherein the contact hole exposes both the impurity diffusion region and the portion of the etch stop spacer adjacent to the exposed impurity diffusion region.

17. The method according to claim 11, wherein the etch stop spacer is partially etched.